AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method of making semiconductor device packages, comprising:

forming a plurality of conductive traces in contact with a top surface of an integral dielectric substrate, the plurality of conductive traces being located on said substrate in correspondence with a plurality of semiconductor devices in a wafer;

subsequently, forming a layered assembly by attaching [[a]] said wafer to said integral dielectric substrate, such that said plurality of conductive traces are in electrical communication with said plurality of semiconductor devices in said wafer;

forming input/output devices in contact with said conductive traces;

testing semiconductor devices in said wafer; and

subsequently, dicing said layered assembly.

2. (Previously presented) The method of claim 1, further comprising the step of connecting said semiconductor devices to said input/output devices.

3. (Original) The method of claim 2, wherein said testing is conducted through said input/output devices.

4. (Original) The method of claim 3, further comprising the step of discarding one or more defective packages.

5. (Currently amended) The method of claim 1, wherein said step of forming said layered assembly ~~includes~~ comprises the step of adhering said wafer to said integral dielectric substrate.

6. (Currently amended) The method of claim 5, further comprising the step of electrically connecting said semiconductor devices to ball grid arrays on said integral dielectric substrate.

7. (Currently amended) The method of claim 6, wherein said connecting step comprises the step of locating wire bonds in openings through said integral dielectric substrate.

8. (Currently amended) The method of claim 6, wherein said connecting step comprises the step of connecting solder bumps on said wafer to circuit traces on said integral dielectric substrate.

9. (Original) The method of claim 6, wherein said dicing step is performed by a saw.

10. (Original) The method of claim 6, further comprising the step of providing a metal layer in said layered assembly.

11. (Currently amended) A method of making semiconductor device packages, comprising:

providing a plurality of conductive structures in contact with a top surface of an integral dielectric substrate, the plurality of conductive structures being located on said substrate in correspondence with a plurality of semiconductor devices in a semiconductor wafer;

subsequently, forming a layered assembly by attaching [[a]] said semiconductor wafer and a stiff metal layer to said integral dielectric substrate with said conductive structures electrically connecting with said semiconductor devices;

placing ball grid arrays in contact with said conductive structures;

electrically connecting said plurality of semiconductor devices in said semiconductor wafer to said ball grid arrays;

determining whether ~~the~~ said semiconductor wafer contains a defective semiconductor device; and

subsequently, dicing said layered assembly.

12. (Currently amended) The method of claim 11, wherein said forming step comprises the step of adhering said semiconductor wafer to said metal layer.

13. (Currently amended) The method of claim 11, wherein said connecting step comprises the step of locating wire bonds in openings in said integral dielectric substrate.

14. (Currently amended) The method of claim 13, further comprising the step of connecting said wire bonds to conductive traces on said integral dielectric substrate.

15. (Currently amended) The method of claim 11, wherein said connecting step comprises the step of connecting solder bumps on said semiconductor wafer to conductive traces on said integral dielectric substrate.

16. (Currently amended) The method of claim 15, further comprising the step of connecting said conductive traces to conductive vias extending through said integral dielectric substrate.

17. (Original) The method of claim 11, wherein said dicing step is performed by a saw.

18. (Original) The method of claim 11, further comprising the step of testing said semiconductor devices through said ball grid arrays.

19. (Currently amended) A method of making semiconductor device packages, comprising:

simultaneously aligning a plurality of semiconductor devices in a semiconductor wafer with respect to a plurality of pre-existing openings in a dielectric tape, before attaching said semiconductor wafer to said dielectric tape;

subsequently, attaching said semiconductor wafer to said dielectric tape;

connecting said semiconductor devices in said semiconductor wafer to ball grid arrays on said dielectric tape; and

simultaneously dicing said semiconductor wafer and said dielectric tape.

20. (Currently amended) The method of claim 19, wherein said semiconductor wafer is optically aligned with respect to said dielectric tape.

21. (Currently amended) The method of claim 19, wherein said semiconductor wafer is magnetically aligned with respect to said dielectric tape.

22. (Currently amended) The method of claim 21, wherein oppositely charged magnetic elements are provided on said semiconductor wafer and said dielectric tape.

23. (Original) The method of claim 21, further comprising the step of locating a magnetic ring in a charged slot.

Claims 24-34. (Canceled)

35. (Currently amended) A method of handling a plurality of semiconductor devices arrayed in a semiconductor wafer, comprising:

adhering said semiconductor wafer to an integral flexible substrate, said integral flexible substrate comprising a plurality of ball grid arrays corresponding with said plurality of semiconductor devices;

connecting said semiconductor devices to respective ball grid arrays located on said integral flexible substrate;

testing said semiconductor devices through said ball grid arrays; and

subsequently, singulating packages from said semiconductor wafer and said integral flexible substrate, such that edges of each piece of said singulated semiconductor wafer and each piece of said singulated flexible substrate are aligned with each other.

36. (Canceled)

37. (Canceled)

38. (Currently amended) The method of claim 41, further comprising the step of segregating said defective packages from other packages.

39. (Currently amended) The method of claim 19, ~~further comprising the~~ wherein said step of attaching said semiconductor wafer to said dielectric tape ~~to said wafer by~~ comprises applying heat or pressure to the assembly.

40. (Currently amended) The method of claim 19, wherein the step of attaching said semiconductor wafer to said dielectric tape comprises ~~further comprising the step of~~ evacuating gas from said assembly.

41. (Previously presented) The method of claim 35, further comprising the step of identifying defective packages.